



IN THE UNITED STATES  
PATENT AND TRADEMARK OFFICE

AF/2816

PATENT APPLICATION

Eduard Sackinger

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SEP -5 2001  
TECHNOLOGY CENTER 2800

CASE 8

Serial No. 09/498,559

Group Art Unit 2816

Filed February 4, 2000

Examiner D. Le

Title Active Inductor

ASSISTANT COMMISSIONER FOR PATENTS  
WASHINGTON, D.C. 20231

SIR:

Enclosed is an amendment in the above-identified application.

NO ADDITIONAL FEE REQUIRED

In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 12-2325** as required to correct the error.

Respectfully,

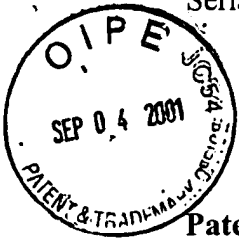
Eugene J. Rosenthal, Attorney  
Reg. No. 36,658  
908-582-4323.

Date: August 31, 2001

Docket Administrator (Room 3J-219)  
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Patent Application

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*H9/Response  
(WE)*

*9/10/01*

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THE COMMISSIONER OF PATENTS AND TRADEMARKS  
WASHINGTON, D.C. 20231  
SIR:

RESPONSE AFTER FINAL REJECTION

This communication is in response to the Office Action dated July 10, 2001.

Remarks

Claims 1-19 are pending in the application.

Claims 16-17 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by United States Patent No. 5,821,825 issued to Kobayashi on October 13, 1998.

Claims 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi.

Each of the various rejections and objections are overcome by amendments which are made to the specification, drawing, and/or claims, as well as, or in the alternative, by various arguments which are presented.

Examiner D. Le and applicant's undersigned representative held a telephone interview on August 30, 2001. Applicant would like to thank the Examiner for his time. The invention, language of the claims, and the technology of Kobayashi was discussed.

**Rejection Under 35 U.S.C. 102(b)**

Claims 16-17 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by United States Patent No. 5,821,825 issued to Kobayashi on October 13, 1998.

The Office Action states that FIG. 2 of Kobayashi discloses an active inductor (22) biased by the voltage divider (R3, R4) which provides a reference voltage between the voltage Vee and ground or beyond the Vee.

This ground of rejection is respectfully traversed for the following reasons.

In Kobayashi, Vee and ground are the voltages supplied by the power supply of Kobayashi, and so, as will be readily recognized by those of ordinary skill in the art, Vee and ground form the range of the DC supply voltage for the Kobayashi circuit. As previously stated, as is well known, according to basic electrical engineering principles, the voltage at the middle of a voltage divider will be a value that is between the values at the ends of the divider. Thus, notwithstanding the Office Action statement to the contrary, since the voltage divider cited by the Office Action is connected between Vee and ground, the bias voltage produced by the Kobayashi voltage divider of R3 and R4 must be between Vee and ground. Consequently, the Kobayashi arrangement does not operate as does applicants' independent claim 16, in that the active inductor of Kobayashi is **not** biased using a voltage generated on said integrated circuit that is **beyond** the range of the voltage supplied by a power supply for operating the integrated circuit. Instead, the Kobayashi arrangement operates to bias its active inductor using a voltage generated on said integrated circuit that is **within** the range of the voltage supplied by a power supply for operating the integrated circuit.

During the interview the Examiner seemed concerned that the language "said active inductor is biased using a voltage generated on said integrated circuit that is beyond the range of the voltage supplied by a power supply for operating said integrated circuit" of claim 16 was unclear, or somehow could be read onto the disclosure of Kobayashi. Furthermore, the Examiner seemed to feel it was possible that there were other voltages supplied to the integrated circuit of Kobayashi besides Vee and ground.

In regards to these concerns, applicant notes that "the range of the voltage supplied by a power supply for operating said integrated circuit" is a phrase which refers

to the limits of the set of voltages that the power supply is supplying to the integrated circuit. Thus, if the lowest voltage supplied to the integrated circuit is X, and the highest voltage supplied is Y, then any voltage including and between X and Y is within the range of the voltage supplied by the power supply. For example, X may be ground (0 volts) and Y may be 5 volts, X may be -12 volts and Y may be ground (0 volts), or X may be -5 volts and Y may be 3 volts. No matter what the particular values of X and Y are, being within the range is to have a voltage equal to or greater than X and less than or equal to Y, while being beyond the voltage range is to have a voltage lower than X or higher than Y.

One should not confuse the tolerance of voltages often given with real world power supplies, which was mentioned by the Examiner, with the values of X and Y. Such tolerances simply tell you how close the actual voltages generated by a power supply will be to the nominally specified values of X and Y. However, with regard to the invention, for any given power supply, it is the actual generated values of X and Y that are of concern, not the nominally specified values.

Consequently, making a determination as to whether an arrangement meets the terms of applicant's claims is very easy. This because, if one needs to determine if "said active inductor is biased using a voltage generated on said integrated circuit that is beyond the range of the voltage supplied by a power supply for operating said integrated circuit", as required by claim 16, one simply needs to look at the voltage biasing the active inductor and compare that voltage to the actual voltages supplied by the power supply, which defines the range of voltage supplied by the power supply. If the voltage biasing the active inductor is less than the actual lowest voltage supplied by the power supply to the integrated circuit, or the voltage biasing the active inductor is greater than the actual highest voltage supplied by the power supply to the integrated circuit, then the active inductor is biased using a voltage generated on the integrated circuit that is beyond the range of the voltage supplied by the power supply and the recitation of applicant's claim 16 is met. On the other hand, if the voltage biasing the active inductor is the same as or greater than the actual lowest voltage supplied by the power supply to the integrated circuit and the voltage biasing the active inductor is less than or equal to the actual

highest voltage supplied by the power supply to the integrated circuit, then the active inductor is biased using a voltage generated on the integrated circuit that is within the range of the voltage supplied by the power supply and the recitation of applicant's claim 16 is not met.

Applying the foregoing to the Examiner's concern that perhaps there were other voltages supplied to the integrated circuit of Kobayashi besides Vee and ground—of which there is no suggestion in Kobayashi—it is clear that even if there were additional voltages supplied to the integrated circuit of Kobayashi, nevertheless applicant's claims would be allowable over Kobayashi. This is because the inductor of Kobayashi is clearly biased by a voltage between Vee and ground, which is within the range of the voltage supplied by the power supply of Kobayashi since, as agreed by the Examiner during the telephone interview, the voltage at the node between R3 and R4 of Kobayashi is greater than Vee and less than ground, and such voltages are actually supplied by the Kobayashi power supply. Thus, the voltage at the biasing voltage of Kobayashi is within the range of voltages supplied by the Kobayashi power supply, not beyond the range, as required by applicant's claims.

In fact, not only is the biasing voltage of Kobayashi within the range of Vee and ground, the only voltages clearly supplied by the power supply of Kobayashi, there is no suggestion in Kobayashi that any other voltages exist in the system. Furthermore, even if there were other voltages supplied to the integrated circuit by the power supply, e.g., a voltage greater than ground or less than Vee, such a voltage would not affect the value of the voltage at the node between R3 and R4 which would still be within, and not beyond the range of voltage supplied by the power supply, because that value would still be greater than Vee and less than ground. In fact, since the range of the voltage supplied by the power supply is, at best, extended by the Examiner's proposed additional voltage, the voltage at the node between R3 and R4 becomes "more" within the range, rather than becoming beyond the range.

Additionally, even if another voltage less than Vee or greater than ground was supplied by the power supply in Kobayashi, which, again, applicant notes there is no such voltage, by not employing such a voltage to bias the inductor Kobayashi teaches away

from applicant's invention, because to not employ such a voltage teaches that even if a voltage beyond what the maximum voltage can be across the inductor exists, one should not use it, but instead one should only use a voltage within the range supplied by the power supply to the inductor.

Further note that applicant's claim 16 requires that the voltage beyond the range of the power supply be generated on the integrated circuit itself. This limitation cannot be taught or made obvious by an additional voltage supplied by the power supply as was suggested by the Examiner.

Therefore, Kobayashi does not teach or suggest applicant's independent claim 16, and applicant's claim 16 is allowable over Kobayashi.

Since claims 17 and 19 depend on and include all the limitations of claim 18, which is allowable over Kobayashi, claims 17 and 19 are also allowable over Kobayashi

**Rejection Under 35 U.S.C. 103(a)**

Claims 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi.

Applicant respectfully traverses this ground of rejection for the following reasons.

This rejection is predicated on the rejection under 35 U.S.C. 102(b) of independent claim 16 on which claim 18 depends being maintainable, since the Office Action essentially repeats the 35 U.S.C. 102(b) rejection and adds that although Kobayashi does not disclose the transistor being PMOS, as recited in claim 18, it would have been obvious to use a PMOS transistor. However, since applicant has shown hereinabove that the rejection of claim 16 under 35 U.S.C. 102(b) cannot be maintained, the rejection of claim 18 under 35 U.S.C. 103 also cannot be maintained.

Thus, applicant's invention is not suggested by Kobayashi and is not merely a design expedient. As a result, applicant's claims are allowable over Kobayashi under 35 U.S.C. 103(a).

Conclusion

It is respectfully submitted that the Office Action's rejections have been overcome and that this application is now in condition for allowance. Reconsideration and allowance are, therefore, respectfully solicited.

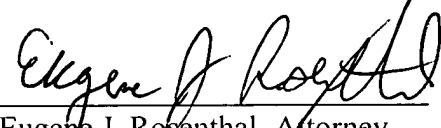
If, however, the Examiner still believes that there are unresolved issues, he is invited to call applicant's attorney so that arrangements may be made to discuss and resolve any such issues.

In the event that an extension of time is required for this amendment to be considered timely, and a petition therefor does not otherwise accompany this amendment, any necessary extension of time is hereby petitioned for, and the Commissioner is authorized to charge the appropriate cost of such petition to the **Lucent Technologies Deposit Account No. 12-2325**.

Respectfully,

Eduard Sackinger

By

  
Eugene J. Rosenthal, Attorney  
Reg. No. 36,658  
908-582-4323

Lucent Technologies Inc.

Date: August 30, 2001